EPC eGaN® FETs Reliability Testing: Phase 10

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The rapid adoption of Efficient Power Conversion (EPC) Corporation's eGaN® devices in many diverse applications, calls for continued accumulation of reliability statistics and research into the fundamental physics of failure in GaN devices. This Phase 10 reliability report adds to the growing knowledge base published in the first nine reports [1-9] and covers several key new topics.

In the first section, we report on the successful completion of automotive AEC-Q101 qualification on four new automotive eGaN® products, with several more in the pipeline for release. AEC-Q101 demands the highest level of reliability standards for power FETs, requiring not only zero datasheet failures, but also low parametric drift during stress testing. We present in detail the test matrix that was completed to achieve this qualification.

Because GaN is a new semiconductor technology compared to traditional Si MOSFETs, many customers request additional testing beyond AEC-Q101 standards, as well as a deeper understanding of the unique mechanisms that could lead to device failures. In the remainder of this report, we turn to several examples of this kind of additional testing.

Section 2 is devoted to the reliability of eGaN FETs under hard and soft switching conditions at high input voltages (V_{IN}). Using a novel test system developed at EPC, we measure $R_{DS(on)}$ with parts operating in switching conditions, and can extrapolate any increases in $R_{DS(on)}$ (also called "dynamic $R_{DS(on)}$") over 10 years of continuous operation. After describing the test system, we examine switching reliability against three acceleration factors: (1) V_{IN}, (2) temperature and, (3) switching frequency.

In Section 3, we turn to the topic of accelerated gate stress testing. Expanding upon the gate reliability studies discussed in Phase 6 report [6], we have developed novel test hardware that allows populations of parts to be tested under DC gate stress, while allowing each part to be continuously monitored in time during the stress duration. Not only is gate leakage monitored continuously, but other device parameters (V_{TH} and I_{DSS}) can be logged on regular intervals. This kind of data gives a more complete picture of device degradation under high gate stress conditions and provides visibility to multiple independent physical failure mechanisms. We provide failure statistics for a wide range of gate bias and temperature conditions and use the results to derive the dominant acceleration factor and activation energy for gate failure.

In Appendix A is a tabular summary of qualification testing results for over 30,000 parts and 18 million device hours tested by EPC.

SECTION 1: AEC-Q101 QUALIFICATION OF eGaN AUTOMOTIVE FETs

In 2018, EPC released four new automotive grade eGaN® FETs: EPC2206, EPC2212, EPC2202, and EPC2203. These parts were qualified in accordance with the component level AEC-Q101 (Rev D1) requirements [10]. All testing requirements and specifications were followed exactly. All four of these automotive devices are compared in Table 1 below. EPC2206 represents the largest die size in the family, with lowest $R_{DS(on)}$. Currently, four additional AEC-grade FETs are in the pipeline for release, ranging in voltage from 40 V up to 200 V.

Part Number	Max V_{DS} (V)	Max V_{GS} (V)	Max $R_{DS(on)}$ (mΩ)	Die Size (mm x mm)	Max Operating Temperature (°C)
EPC2206	80	6	2.2	XL (6.05 x 2.3)	150
EPC2212	100	6	13.5	M (2.11 x 1.63)	150
EPC2202	80	5.75	17	M (2.11 x 1.63)	150
EPC2203	80	5.75	80	S (0.95 x 0.95)	150

Table 1: Initial EPC 80 V/100 V Automotive Product Family

Qualification Test Overview

EPC's EPC2206, EPC2202, EPC2203 and EPC2212 eGaN FETs were subjected to a wide variety of stress tests following the specifications of AEC-Q101 (Rev D1) developed for silicon-based power MOSFETs. These tests include:

- Moisture sensitivity level 1 (MSL1): Parts are subjected to high moisture and temperature. MSL1 is the most stringent of the moisture sensitivity levels, requiring 85°C and 85% humidity for 168 hours.
- Preconditioning: Parts undergo the following steps in sequence: (1) 125°C bake for a minimum of 24 hours; (2) MSL1; (3) 3 times reflow.
- Parametric Verification: Device parameters are measured at -40°C, 25°C, and 150°C to ensure compliance with datasheet limits over the entire temperature range.
- Electrostatic Discharge (ESD) Characterization: Parts are tested under both Human Body Model (HBM) and Charged Device Model (CDM) to assess device susceptibility to electrostatic discharge events.

– High temperature reverse bias (HTRB): Parts are subjected to a drain-source voltage at the maximum rated temperature and maximum rated voltage.

– High temperature gate bias (HTGB): Parts are subjected to a gate-source voltage at the maximum rated temperature and maximum rated gate voltage.

– Unbiased highly accelerated test (uHAST): Parts are stressed in a non-condensing humid environment for 96 hours at 130°C, 85% humidity, and a vapor pressure of 33.3 psia.

– Temperature cycling (TC): Parts are subjected to alternating high and low temperature extremes from -55°C to 150°C for a total of 1000 cycles.

– High temperature, high humidity reverse bias (H3TRB): Parts are subjected to 1000 hours of 85°C, 85% humidity with the drain biased at 80% of the maximum rating.

– Intermittent Operating Life (IOL): Parts are temperature cycled with a short cycle period (6 minutes) and device heating occurred through internal electrical power dissipation.

– Destructive Physical Analysis: Parts are delayered and physically analyzed looking for defects resulting from stress testing.

For most of the required tests, the full sample population of 77 parts x 3 lots were used for every device. In some cases, however, we followed a matrix (or similarity) qualification approach by combining data from devices within the same package or voltage family.

All devices put on test as part of this qualification underwent external visual inspection prior to test. This microscope inspection checks for physical damage to the chip-scale package, such as edge chipping or cracks, that may have resulted from assembly or transit. Damaged parts are removed from the test population.

For all qualification tests, the stability of the devices is verified with DC electrical tests before and after stress. In many cases, interim readouts are also performed. Electrical parameters are measured at room temperature. The parameters include: gate-source threshold voltage (V_{TH}), on-state resistance $R_{DS(on)}$, off-state drain leakage (I_{DSS}), and gate leakage (I_{GSS}). For V_{TH} and $R_{DS(on)}$, a failure is recorded when either of the following occurs: (i) the measurement exceeds the datasheet specifications; or (2) the measurement has changed by more than 20% of its initial value. For I_{DSS} and I_{GSS}, a failure is recorded if the measurement exceeds datasheet limit, or if it has increased by more than 5x during test.

For certain qualification tests, parts were mounted onto high Tg FR-4 (FR-5 or NP-175) or polyimide (Arlon 85NT) PCB adaptor cards. These cards simplify the process of post-screening and electrically stressing the parts. Adaptor cards (1.6 mm in thickness) with two copper layers were used. The top copper layer was 1 oz. or 2 oz., and the bottom copper layer was 1 oz. Kester NXG1 type 3 SAC305 solder no clean flux was used in mounting the part onto an adaptor card. After assembly, parts were either baked or flux-cleaned.

For other qualifications tests, including MSL1 and TC, parts were not mounted to adaptor cards. Electrical tests were performed using probe needles touching the solder pads of the bare die.

The distinct physics of failure of eGaN devices compared to MOSFETs requires further study in order to confidently project service life based on accelerated stress testing. In these cases, EPC takes a three-prong approach to help customers gain confidence that the reliability needs of their mission profile will be met:

1) EPC conducts standard AEC-Q101 qualification of eGaN FETs, following all requirements and standards exactly. This establishes a reliability baseline.

2) EPC conducts accelerated voltage and/or temperature studies, allowing us to study intrinsic (fundamental) failure modes and project lifetime within the datasheet operating range. An example of this kind of study is provided in Section 3, where we focus on gate reliability.

3) EPC conducts additional operating life testing in test circuits that emulate the stress conditions seen in the application environment. Examples include both lidar and DC-DC conversion. These tests are often designed and implemented in cooperation with end-users. The tests are designed to directly verify that the service life of the eGaN product will exceed automotive mission requirements (ranging from 15000 hours up to 25 years of continuous operation). Operating life data of this type is not presented in this document but is available upon request from EPC.

High Temperature Reverse Bias (HTRB)

Parts were subjected to 100% of the rated drain-source voltage at the maximum operating temperature (150°C) for a stress period of 1000 hours, satisfying AEC-Q101 requirements for a 150°C rating. As shown in Table 2 below, three separate lots of 77 parts were tested for each product.

Parts were mounted on high Tg FR-4 adapter cards. Testing was conducted in accordance with MIL-STD-750-1 (M1038 Method A) [11]. This standard requires the parts to be under bias during temperature ramp up and cool down. In addition, post-screening must occur within 24 hours after bias has been removed.

Stress Test	Part Number	Max V_{DS} (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTRB	EPC2206	80	M (2.11 x 1.63)	T = 150°C, V_{DS} = 80 V	0	77 X 3	1000
HTRB	EPC2212	100	S (0.95 x 0.95)	T = 150°C, V_{DS} = 100 V	0	77 X 3	1000
HTRB	EPC2202	80	M (2.11 x 1.63)	T = 150°C, V_{DS} = 80 V	0	77 X 3	1000
HTRB	EPC2203	80	S (0.95 x 0.95)	T = 150°C, V_{DS} = 80 V	0	77 X 3	1000

Table 2. High Temperature Reverse Bias Test

High Temperature Gate Bias (HTGB)

Parts were subjected to maximum-rated gate-source bias at the maximum operating temperature (150°C) for a stress period of 1000 hours. A sample size of 3 lots x 77 parts was tested for each product. The number of lots, test duration and temperature satisfy the AEC-Q101 requirements for a 150°C rating.

Parts were mounted on high Tg FR-4 adapter cards. Testing was conducted in accordance with JESD22-A108 [12]. This standard requires the parts to be under bias during temperature ramp up and cool down. In addition, post-screening must occur within 96 hours after bias has been removed.

Stress Test	Part Number	Max V_{GS} (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTGB	EPC2206	6.0	XL (6.05 x 2.3)	T = 150°C, V_{GS} = 6.0 V	0	77 x 3	1000
HTGB	EPC2212	6.0	M (2.11 x 1.63)	T = 150°C, V_{GS} = 6.0 V	0	77 x 3	1000
HTGB	EPC2202	5.75	M (2.11 x 1.63)	T = 150°C, V_{GS} = 5.75 V	0	77 x 3	1000
HTGB	EPC2203	5.75	S (0.95 x 0.95)	T = 150°C, V_{GS} = 5.75 V	0	77 x 3	1000

Table 3. High Temperature Gate Bias Test

Unbiased Highly Accelerated Test (uHAST)

Parts were subjected to 96 hours at a temperature of 130°C, relative humidity of 85%, and a vapor pressure of 33.3 psia. As summarized in Table 4 below, three lots of EPC2206, EPC2202 and EPC2203 completed testing. EPC2212, which shares an identical package to EPC2202, was qualified by matrix.

All parts were mounted on high Tg FR-4 (NP-175) adaptor boards. Per AEC requirements, all parts went through pre-conditioning before uHAST. Testing was conducted in accordance with the JESD22-A118 standard [13].

Stress Test	Part Number	Max V_{DS} (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
uHAST	EPC2206	80	XL (6.05 X 2.3)	T = 130°C, RH = 85%, VP = 33.3 psia	0	77 X 3	96
uHAST	EPC2202	80	M (2.11 x 1.63)	T = 130°C, RH = 85%, VP = 33.3 psia	0	77 X 3	96
uHAST	EPC2203	80	S (0.95 x 0.95)	T = 130°C, RH = 85%, VP = 33.3 psia	0	77 X 3	96

Table 4. Unbiased Highly Accelerated Test

Temperature Cycling (TC)

Parts were subjected to temperature cycling between -55°C and +150°C for a total of 1000 cycles. A minimum of 5 minutes dwell time and 2-3 cycles per hour were used in accordance with the JEDEC Standard JESD22A104 Condition B [14]. All parts that are in bare die format or mounted on FR5 went through pre-conditioning prior to TC.

As seen in Table 5, three lots of the largest die EPC2206 passed 1000 cycles, with bare die (package) loaded into trays, satisfying the AEC requirement. In addition, one lot of 48 parts passed 1000 cycles on low-CTE polyimide PCB (Arlon 85NT). For EPC2202 and EPC2203, qualification was also achieved in bare die format. Supplemental testing on PCB's (Arlon 85NT and FR5) is also provided in the table. EPC2212 was qualified by matrix with EPC2202.

Stress Test	Part Number	Max V_{DS} (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)	Format
TC	EPC2206	80	XL (6.05 x 2.3)	-55 to 150°C, Air	0	77 x 3	1000	Bare Die
TC	EPC2206	80	XL (6.05 x 2.3)	-55 to 150°C, Air	0	48 x 1	1000	PCB (Arlon 85NT)
TC	EPC2202	80	M (2.11 x 1.63)	-55 to 150°C, Air	0	77 x 3	1000	Bare Die
TC	EPC2203	80	S (0.95 x 0.95)	-55 to 150°C, Air	0	77 x 3	1000	Bare Die
TC	EPC2202	80	M (2.11 x 1.63)	-55 to 150°C, Air	0	77 x 2	1000	PCB (Arlon 85NT)
TC	EPC2202	80	M (2.11 x 1.63)	-55 to 150°C, Air	0	77 x 2	500	PCB (FR5)
TC	EPC2203	80	S (0.95 x 0.95)	-55 to 150°C, Air	0	77 x 2	500	PCB (FR5)

Table 5. Temperature Cycling Test

High Temperature High Humidity Reverse Bias (H3TRB)

Parts were subjected to a drain-source bias of 80% maximum voltage rating, 85% RH and 85°C for a stress period of 1000 hours. The testing was done in accordance with the JEDEC Standard JESD22-A101 [15], as required by AEC-Q101. All parts were mounted on FR4 adaptor boards. All parts went through pre-conditioning before H3TRB. Test results are summarized in Table 6. All parts passed 1000 hours stress with sample size meeting or exceeding AEC-Q101 requirements.

Stress Test	Part Number	Max V_{DS} (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
H3TRB	EPC2206	80	XL (6.05 x 2.3)	T = 85°C, RH = 85%, V_{DS} = 64 V	0	77 x 3	1000
H3TRB	EPC2212	100	M (2.11 x 1.63)	T = 85°C, RH = 85%, V_{DS} = 80 V	0	77 x 3	1000
H3TRB	EPC2202	80	M (2.11 x 1.63)	T = 85°C, RH = 85%, V_{DS} = 64 V	0	77 x 5	1000
H3TRB	EPC2203	80	S (0.95 x 0.95)	T = 85°C, RH = 85%, V_{DS} = 64 V	0	77 x 3	1000

Table 6. High Temperature High Humidity Reverse Bias Test (H3TRB)

Moisture Sensitivity Level 1 (MSL)

MSL1 test results are summarized in Table 7. Parts were subjected to 85% RH at 85°C for a soak period of 168 hours. These conditions correspond to a moisture sensitivity level 1, the most stringent level of moisture sensitivity testing. For this testing, devices were either attached to PCB test coupons, or tested in bare die format. (For bare die, pre-screen and post-screen were performed using probe needles to contact the solder pads of the bare die). As can be seen in the table, in either PCB or bare die format, all parts pass AEC requirements for MSL1.

Stress Test	Part Number	Max V_{DS} (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)	Format
MSL1	EPC2206	80	XL (6.05 x 2.3)	T = 85°C, RH = 85%, 3x reflow	0	77 x 4	168	PCB (FR-4)
MSL1	EPC2206	80	XL (6.05 x 2.3)	T = 85°C, RH = 85%, 3x reflow	0	77 x 3	168	Bare Die
MSL1	EPC2202	80	M (2.11 x 1.63)	T = 85°C, RH = 85%, 3x reflow	0	77 x 3	168	Bare Die
MSL1	EPC2203	80	S (0.95 x 0.95)	T = 85°C, RH = 85%, 3x reflow	0	77 x 3	168	Bare Die

Table 7. Moisture Sensitivity Level 1 Verification Testing

Destructive Physical Analysis

In accordance with AEC-Q101 requirements, two parts from each product were selected for physical analysis after successfully completing uHAST testing. The physical analysis was conducted in three steps: (1) removal of die from PCB adapter card; (2) chemical removal of solder bumps/bars; (3) removal of top-layer passivation layers via chemical etch. After each step, a high magnification optical microscope inspection was performed. No damage or abnormalities were observed resulting from the environmental stress testing.

Electrostatic Discharge (ESD) Sensitivity

EPC2206, EPC2202, and EPC2203 were tested for ESD sensitivity using both the human body model (HBM) and charged device model (CDM). Testing was conducted according to AEC-Q101-001 [17] and AEC-Q101-005 standards [18]. Device parameters were measured before and after ESD testing. Results are shown in Table 8 below. All parts passed CDM with a 1000 V rating. EPC2202 and EPC2206 passed HBM with a 500 V rating; the small die EPC2203 (with smallest input capacitance) passed HBM at 250 V.

Stress Test	Part Number	Max V_{DS} (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)
ESD - HBM	EPC2206	80	XL (6.05 x 2.3)	500 V	0	10 x 1
ESD - HBM	EPC2206	80	XL (6.05 x 2.3)	1000 V	1	10 x 1
ESD - CDM	EPC2206	80	XL (6.05 x 2.3)	1000 V	0	10 x 1
ESD - HBM	EPC2202	80	M (2.11 x 1.63)	500 V	0	10 x 1
ESD - HBM	EPC2202	80	M (2.11 x 1.63)	1000 V	1	10 x 1
ESD - CDM	EPC2202	80	M (2.11 x 1.63)	500 V	0	10 x 1
ESD - CDM	EPC2202	80	M (2.11 x 1.63)	750 V	0	10 x 1
ESD - CDM	EPC2202	80	M (2.11 x 1.63)	1000 V	0	10 x 1
ESD - HBM	EPC2203	80	S (0.95 x 0.95)	250 V	0	10 x 1
ESD - HBM	EPC2203	80	S (0.95 x 0.95)	500 V	1	10 x 1
ESD - CDM	EPC2203	80	S (0.95 x 0.95)	500 V	0	10 x 1
ESD - CDM	EPC2203	80	S (0.95 x 0.95)	750 V	0	10 x 1
ESD - CDM	EPC2203	80	S (0.95 x 0.95)	1000 V	0	10 x 1

Table 8. ESD HBM and CDM Tests

Parametric Verification

In accordance with AEC-Q101 requirements, EPC2206 device parameters were measured at -40°C, 25°C, and 150°C to ensure compliance with datasheet specifications over the entire temperature range. Parametric verification was performed 3 lots x 25 parts, for EPC2206, EPC2212, EPC2202 and EPC2203 with results in Table 9.

Stress Test	Part Number	Max V_{DS} (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)
PV	EPC2206	80	XL (6.05 x 2.3)	T = 40°C, 25ºC, 150°C	0	25 x 3
PV	EPC2212	100	M (2.11 x 1.63)	T = 40°C, 25ºC, 150°C	0	25 x 3
PV	EPC2202	80	M (2.11 x 1.63)	T = 40°C, 25ºC, 150°C	0	25 x 3
PV	EPC2203	80	S (0.95 x 0.95)	T = 40°C, 25ºC, 150°C	0	25 x 3

Table 9. Parametric Verification Tests

Intermittent Operating Life (IOL)

In accordance with MIL-STD-750 (Method 1037) [11], parts are power cycled over a ΔT = 125°C temperature range. Devices are heated through internal electrical power dissipation by biasing them in the linear mode, with combined gate and drain bias, and a regulated drain current. With a one minute temperature ramp, and a five minute cool down, a minimum of 5000 cycles are required. Die were assembled onto low CTE polyimide PCBs (Arlon 85NT). As seen in Table 10, two lots of EPC2202 passed 5000 cycles, and one lot of EPC2203 passed 7500 cycles (exceeding AEC requirements). In addition, one lot (32 parts) of EPC2206 was also tested to 5000 cycles with no failures.

Stress Test	Part Number	Max V_{DS} (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)	Format
IOL	EPC2206	80	XL (6.05 x 2.3)	ΔTj = 125°C; t_{ON} / t_{OFF} = 1 min /5 min	0	32 x 1	5000	PCB (Arlon 85NT)
IOL	EPC2202	80	M (2.11 x 1.63)	ΔTj = 125°C; t_{ON} / t_{OFF} = 1 min /5 min	0	77 x 2	5000	PCB (Arlon 85NT)
IOL	EPC2203	80	S (0.95 x 0.95)	ΔTj = 125°C; t_{ON} / t_{OFF} = 1 min /5 min	0	77 x 1	7500	PCB (Arlon 85NT)

Table 10. Intermittent Operating Life Tests (IOL)

SECTION 2: SWITCHING RELIABILITY TESTING

Recently, the JEDEC JC-70.1 committee released a test guideline for the measurement of dynamic on-resistance ($dR_{DS(on)}$) in GaN based power electronics [19]. The test method uses double-pulse inductive hard-switching. EPC uses this method to characterize eGaN FETs, as reported previously [20].

In addition, EPC has developed an extensive resistive hard-switching test capability, which was specifically designed to characterize $dR_{DS(on)}$ over long term continuous hard and/or soft-switching operation. Figure 1 shows the basic test circuit for this system. It is based on a resistive switching circuit where the Device Under Test (DUT) is hard-switched continuously while measuring and logging $R_{DS(on)}$. The system configuration consists of a motherboard holding the components on Figure 1, except for the DUT, which is mounted on a separate DUT card that plugs into an edge card connector located on the motherboard. An external gate resistor ($R_{G,\ ext}$) is used to slow down the switching transients. The purpose of this resistor is twofold: first to minimize gate voltage overshoot (a consequence of the test configuration and its parasitic inductance), and second to enhance the time with simultaneous high voltage and high current present during hard-switching transitions (accelerating potential $dR_{DS(on)}$ effects).

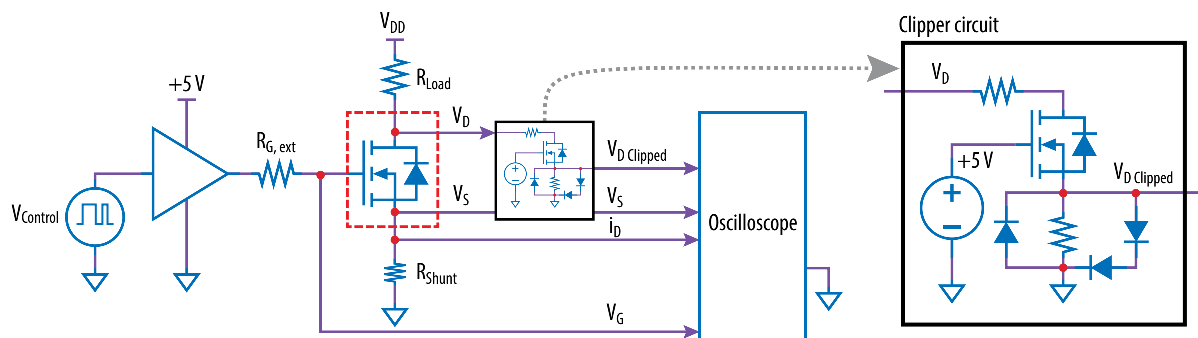


Figure 1. Overall test circuit (left) with zoomed up view of the clipper circuit schematic (right).

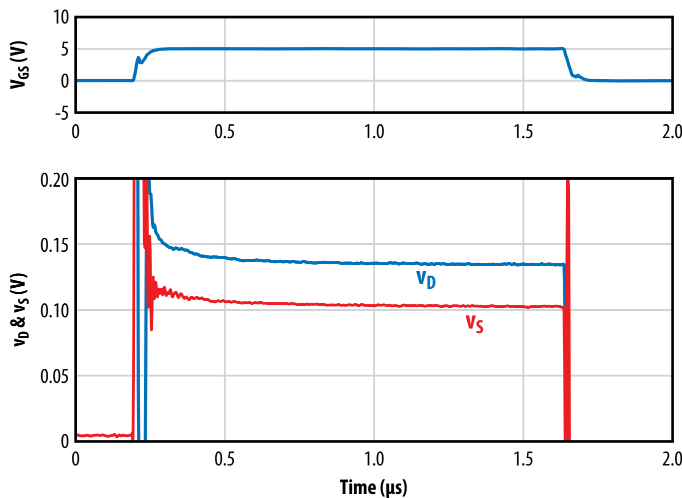
The system is designed to run under multiple operating conditions, including various stress voltages (V_{DD}), switching frequency (f_{sw}), duty cycle (D), and operating temperature as measured at the die's substrate (T_C).

A temperature-controlled system was also developed to evaluate $dR_{DS(on)}$ at specific temperatures. For "hot" tests, the system consists of a power resistor used as a heater, attached to the back of the card where the DUT is mounted. For "cold" tests, it uses a Peltier module mounted directly against the die, with a thermal interface material in between. The amount of power dissipated by the heater or absorbed by the Peltier module is regulated with a proportional-integral (PI) controller that uses the die temperature (T_C) as feedback to ensure that the target temperature is maintained through the test. Note that for "cold" tests, the cooler should be able to keep the die at the desired temperature while absorbing the conduction and switching losses generated during the test.

$R_{DS(on)}$ is calculated from measurements of the drain and source voltages (v_D and v_S), and the current flowing through the DUT during the on-state (i_D). Both drain and source should be Kelvin-sensed to minimize measurement errors. In addition, special attention needs to be paid to measure v_D successfully. Note that during the DUT's off-state $v_D = V_{DD}$, which can be hundreds of volts, whereas during the on-state the voltage drops to a few millivolts ($v_D = R_{DS(on)} \cdot i_D$). Such a small voltage signal requires a fine oscilloscope setting that becomes highly saturated when exposed to the high voltage present during the off-state, leading to incorrect measurements. This issue can be solved with a clipper circuit, whose main function is to disconnect the DUT's drain from the oscilloscope during the off-state (high voltage present) and connect it back during the on-state (low voltage present). Multiple topologies capable of such function are readily available in the literature [20-22]. For the purpose of this study the circuit shown on Figure 1, based on a self-controlled clipper FET, together with some clamping diodes, was used.

Using an oscilloscope, v_D, v_S, and i_D can be captured and recorded at any given time throughout the test. $R_{DS(on)}$ may be calculated offline as shown on Figure 2. This method allows continuous monitoring of $R_{DS(on)}$ for extended periods of time. However, this task becomes a challenge for long test times since temperature-driven drifts in the oscilloscope can distort the measurements. In order to minimize this effect, the same channel settings were used for v_D, v_S, and i_D, so any possible gain drifts cancel out when $R_{DS(on)}$ is calculated (assuming comparable gain drifts over temperature for all channels).

It is good practice to use a control device to verify that the system measures $R_{DS(on)}$ correctly and that the oscilloscope inputs are not saturated. A Si MOSFET with a similar voltage and current rating was used.



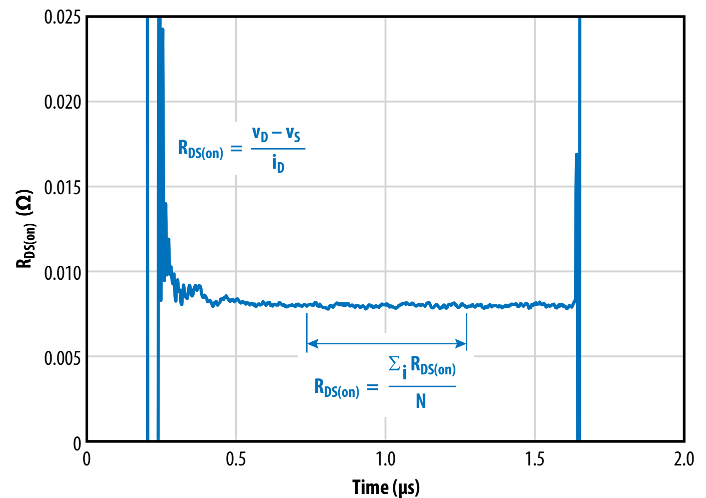


Figure 2: Waveforms of EPC2045 under hard switching conditions

Test Results

The device evaluated is the EPC2045, a 100 V eGaN FET with maximum $R_{DS(on)}$ = 7 mΩ. Table 11 provides a summary of the test conditions used to characterize its long term $dR_{DS(on)}$. These conditions include different voltages, operating temperatures, and switching frequencies. A constant duty cycle of 15% was maintained for all the tests, providing a minimum window of 750 ns (f_{SW} = 200 kHz) to measure $dR_{DS(on)}$. The DUT was driven with TI's LM5114 gate driver and 5 V.

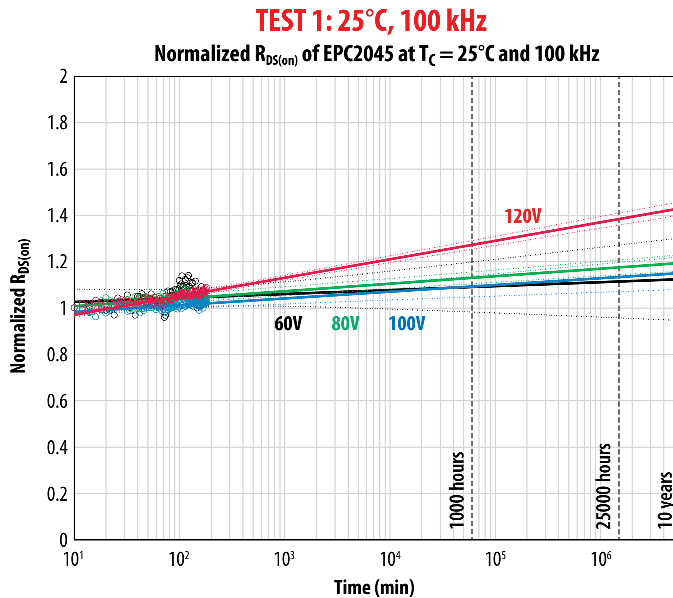
The same device was also tested in [20] using a Double Pulse Test, demonstrating the lack of $dR_{DS(on)}$ within 50 ns of turn-on with up to 100 V and 20 A. This report focuses on the long term $R_{DS(on)}$ stability under continuous hard-switching conditions. For each test, the same device was operated for 3 hours at each voltage while recording $R_{DS(on)}$.

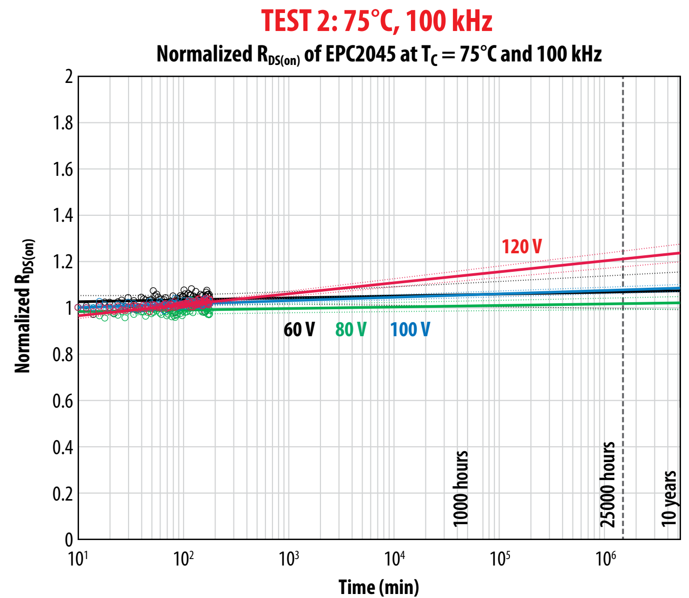
DUT: EPC2045		Frequency (kHz)	
		100	200
Temperature (°C)	25	Test 1: 60 V–120 V	
	75	Test 2: 60 V–120 V	
	125	Test 3: 60 V–120 V	Test 4: 60 V–120 V

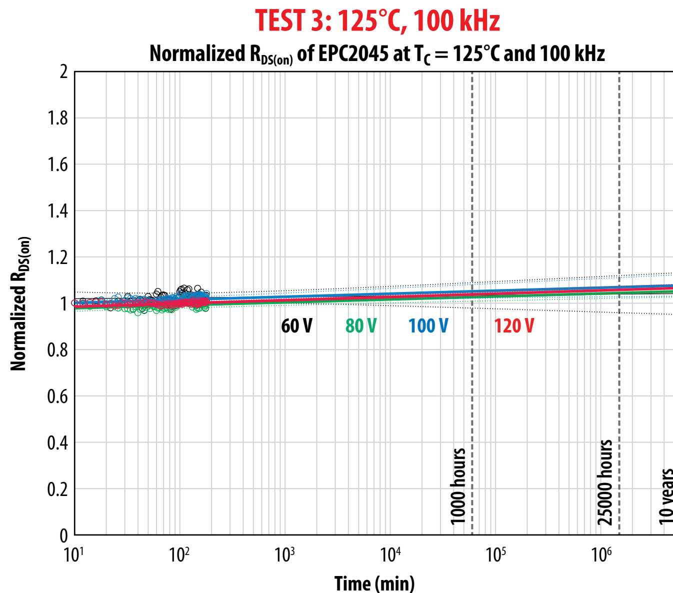
Table 11: Test matrix for $dR_{DS(on)}$ characterization

Figure 3 shows the normalized $R_{DS(on)}$ over time (with horizontal axis in log10 scale) for tests 1-4. Using this representation of the results, it is appropriate to use the 3-hour test to project the accumulated $R_{DS(on)}$ shift after 10 years. Note that this estimate corresponds to 10 years of uninterrupted operation under hard-switching.

Secondly is the effect of voltage on $R_{DS(on)}$. For each test, at each voltage, the die temperature remains constant, which allows us to isolate the cause for $R_{DS(on)}$ shifts. Under these conditions it can be affirmed that shifts are solely caused by electron trapping and not temperature changes. By looking at the nearly flat slopes of the line fits for each test, there is no voltage acceleration up to 100 V, the maximum voltage rating of the part. This statement remains true at all the temperatures and switching frequencies tested. It is beyond the maximum operating voltage of the device (120 V), that $dR_{DS(on)}$ becomes noticeable.







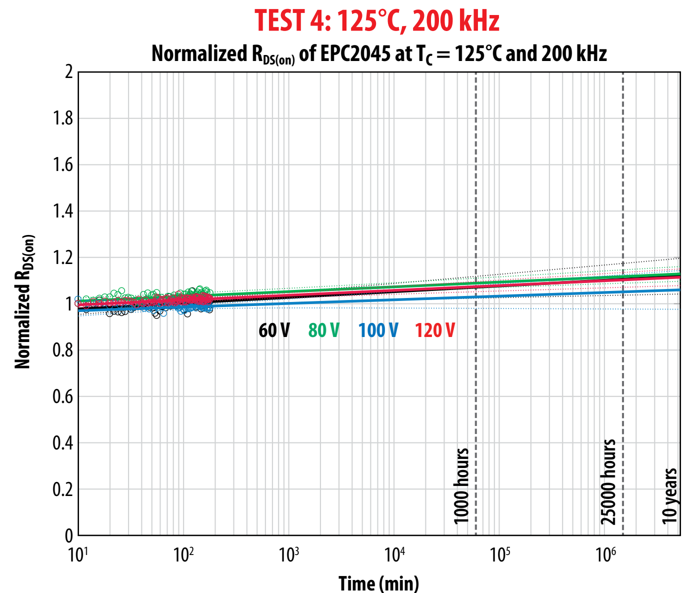


Figure 3: Normalized $R_{DS(on)}$ over time for EPC2045 devices at different temperatures and bias voltages when subjected to hard switching at 100 kHz

At accelerated drain voltage, $dR_{DS(on)}$ in eGaN FETs is caused by hot carrier scattering. Electrons are accelerated by the high electric field, gaining sufficient energy (well above thermal equilibrium) to scatter away from the two-dimensional electron gas (2DEG). These electrons can become trapped near the surface, where negative charge accumulated over time causes an increase in device resistance. This degradation mechanism is similar to the well-studied hot carrier injection (HCI) mechanism seen in silicon MOSFETs [24]; however, the location of the charge trapping is different in eGaN devices. Hot carrier scattering has a negative temperature activation energy. At lower temperatures, the effect becomes more pronounced because electrons can achieve higher energy in an electric field due to reduced phonon scattering.

Figure 4 shows the effect of temperature on $dR_{DS(on)}$ at 120 V. At this voltage level (20% beyond the maximum voltage rating of the device), the long term $R_{DS(on)}$ shift is mitigated at higher operating temperatures, since the slope of line fit decreases with higher temperatures. This negative temperature activation adds compelling evidence that hot carrier scattering is the underlying root cause of $dR_{DS(on)}$.

SECTION 3: GATE RELIABILITY ACCELERATION FACTORS

Gate reliability of eGaN FETs is further examined at different temperatures and voltages well above the maximum ratings of the devices under test. In this section a traditional acceleration factor analysis of eGaN device gates using EPC2212 (AEC qualified) as the test device. Similar results can be expected for all eGaN devices because they share identical internal gate structure. By inducing failures at highly accelerated voltages, and at different temperatures, it is possible to extract a voltage acceleration factor and a temperature activation energy, resulting in a simple mathematical formula customers can use to predict lifetime under their use conditions.

There are several separate physical mechanisms that can contribute to failure during HTGB stress at high gate voltage. These include: (i) dielectric failure; (ii) gate sidewall rupture; (iii) increased off-state drain leakage (I_{DSS}) resulting from loss of gate control; and (iv) V_{TH} shift from charge trapping. Each mechanism has a unique physics of failure, and therefore they cannot all be characterized by a single acceleration factor and activation energy. As a result, all must be monitored over a broad range of temperature and voltage, to determine which mechanisms are dominant under typical use conditions within datasheet limits.

To facilitate this kind of study, EPC developed a custom test system with the ability to monitor multiple device parameters in real time while the parts are under gate stress. The test systems accommodate 32-48 parts at the same time. The parameters are I_{GSS} (gate leakage during voltage stress), threshold voltage (V_{TH}), and I_{DSS} (off-state drain leakage with V_{GS} = 0 V and V_{DS} = 10 V). I_{GSS} is monitored continuously in time during the gate stress period, with 3s readout of every part under test. V_{TH} and I_{DSS} are measured in 30 min intervals by removing gate stress for a short period of time.

Figure 5 shows an example real-time HTGB parametric data from a test consisting of 32 devices with 7.5 V on gate at 25°C. Data for all 32 parts are overlaid in the plots spanning a total of 600 hours test time. As can be seen in the real-time plots, even at 7.5 V (well above datasheet maximum rating of 6 V), no parts suffer gate rupture or any other parametric degradation within the 600-hour test period.

To determine the voltage acceleration of HTGB failure, a matrix of tests was conducted at voltages between 6.5 V and 9.5 V, at the two different temperatures of 25°C and 120°C. Note that this voltage range is well outside of the safe operating range of less than 6 V for eGaN FETs. Each voltage leg consisted of 32 parts, and all 3 parameters were monitored continuously in time, on every device, as described earlier. A failure was defined as any parameter (I_{GSS}, I_{DSS}, V_{TH}) exceeding its datasheet limit.

Below 8 V, no failures were observed in any of experimental legs. At 7.5 V no failures or parametric drift were observed at over 600 hours. This leg will be continued to 2000 hours to check for any latent or slowly evolving degradation mechanisms that might be dominant at a lower gate voltage.

At 8 V and beyond, the dominant failure mechanism is an abrupt increase in gate leakage, phenomenologically similar to time-dependent dielectric breakdown (TDDB) seen in MOSFETs [25].

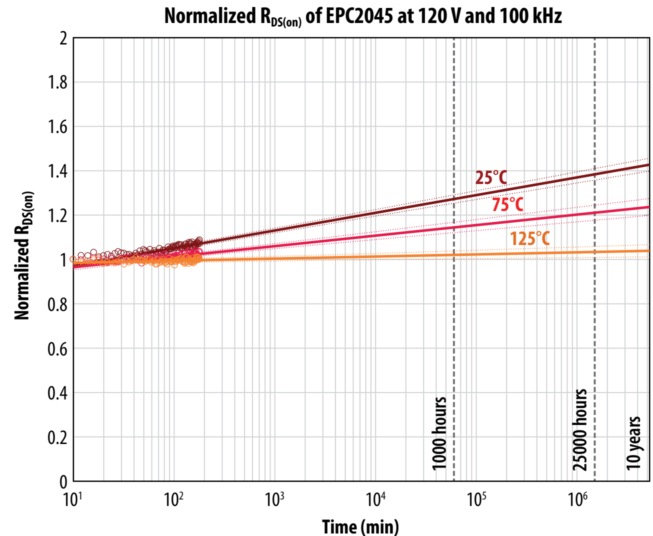


Figure 4: The effect of temperature on $dR_{DS(on)}$ at 120 V for EPC2045 eGaN FET under hard switching conditions at 100 kHz

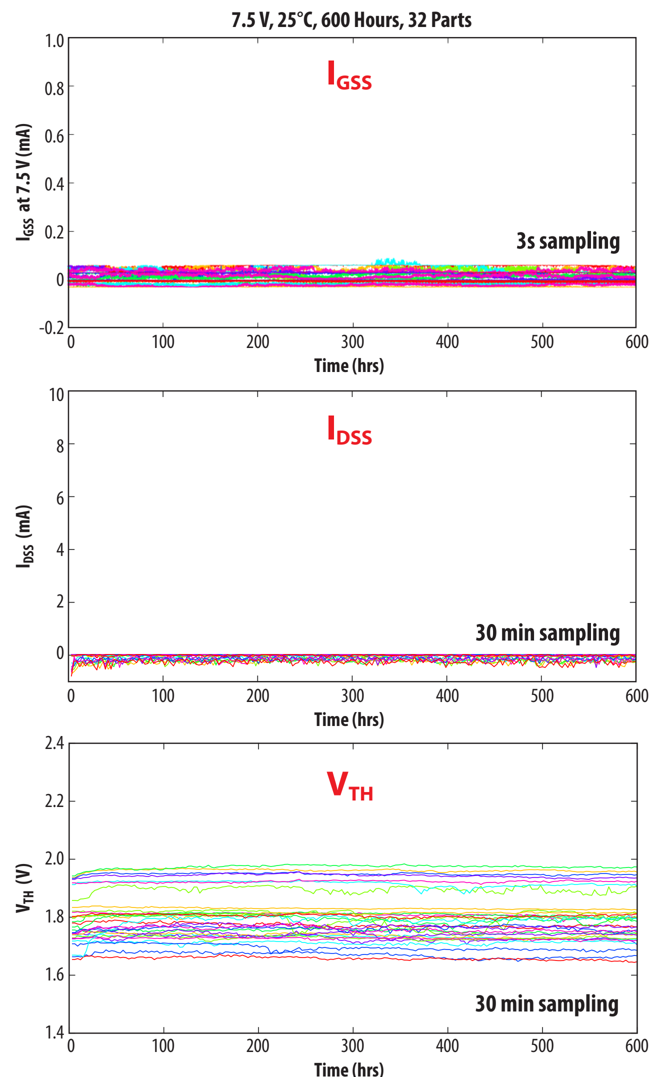


Figure 5: Real-time HTGB parametric data from a test consisting of 32 devices with V_{GS} = 7.5 V at 25°C. Gate leakage at 7.5 V (I_{GSS} in top plot) is sampled for each part every 3 seconds. Data for all 32 parts are overlaid in the plots. The lower plots show I_{DSS} and V_{TH}, sampled every 30 min. As can be seen in the real-time plots, even at 7.5 V (well above the datasheet maximum rating of 6 V), no parts suffer gate rupture or any discernable parametric degradation within the 600-hour test period.

Figure 6 shows examples of two such failures at 8.5 V. The gates are initially normal, but then suffer an abrupt catastrophic increase in gate leakage to the compliance level of the test system. Once the gate ruptures, the damage is permanent, and the device never recovers. The time to failure is a stochastic variable that can be recorded for each device using the time series data provided by our test system. In eGaN FETs this failure mode is likely caused by a breakdown at the pGaN - dielectric interface along the gate sidewall.

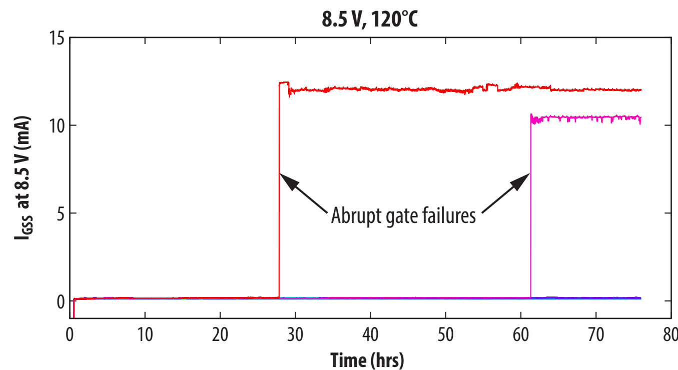


Figure 6: Example of abrupt gate rupture failures in time. Gate leakage versus time for 8 parts shown at the same time. In this time interval, 2 devices suffer time-dependent dielectric breakdown, resulting in gate leakage abruptly jumping up to compliance level.

Figure 7 shows time-to-failure data for different gate voltages and at both temperatures. The data was analyzed using the same methods as described in our earlier Phase 6 reliability report [6]. Raw time to failure was fit to a 2-parameter Weibull distribution for each voltage/temperature leg using maximum likelihood estimation (MLE). The fits are indicated by solid lines in the graphs. The Weibull shape (or slope) parameter was constrained to be the same for all voltage/temperature legs in this study. Though this assumption is ad hoc, it seemed to provide a good fit to all the data. The Weibull scale (or offset) parameter was fit independently for each leg. The dashed lines represent 90% confidence intervals for the scale parameter.

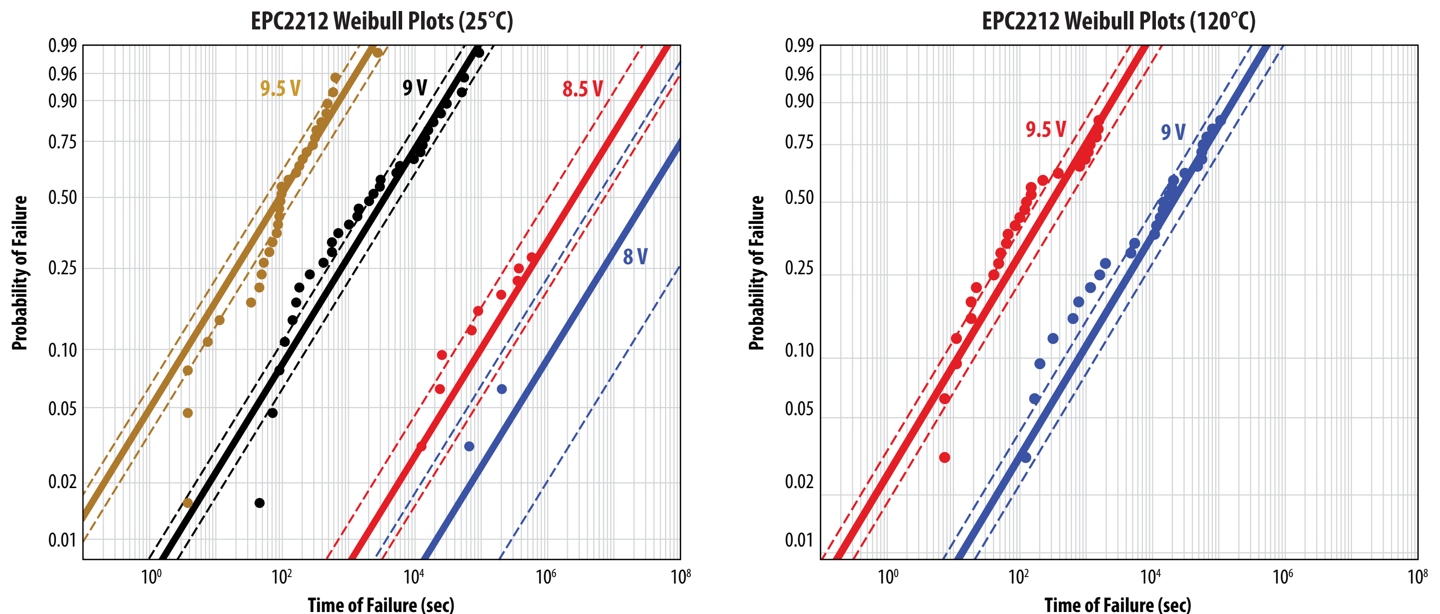


Figure 7: Weibull plots for accelerated gate failures at both 25°C (left) and 120°C (right). Solid lines indicate MLE fits to the 2-parameter Weibull distribution. Note that a common Weibull shape parameter, k, was fit to all the data (all voltages and temperatures). The dashed lines represent 90% confidence intervals on the fit for the Weibull scale parameter λ for all legs in this study.

Figure 8 shows mean time to failure (MTTF) versus gate bias and temperature. Error bars on each data point indicate 90% confidence intervals on the MTTF resulting from the MLE Weibull fit. The dashed lines indicate the best fit to a conventional exponential voltage acceleration function (characterized by parameters A and β shown in the equation at the upper right). A separate fit was performed at 25°C and 120°C. At both temperatures, a strong voltage acceleration factor was found (β = 9.2/V for 25°C), which corresponds to almost 4 orders of magnitude increase in lifetime for every volt drop in gate bias. This acceleration factor is in fairly close agreement with the value found in our earlier study in the Phase 6 report. Though the MTTF was found to be somewhat longer at higher temperature, the difference is small in comparison to the statistical error bars. As a result, we can infer the temperature activation energy of this failure mechanism is near zero ($E_A \approx 0$).

Figure 9 shows the mean time to failure (MTTF) and time to 1 ppm, 10 ppm, and 100 ppm failure ($T_{0.1\%}$) versus gate bias at 25°C. Note that T_{XppM} was calculated using the common Weibull shape parameter for all voltage legs. Green solid lines are the best fit to the simple exponential acceleration function. The acceleration function has been projected back to 5 V to assess gate reliability within the datasheet operating range of this part (< 6 V V_{GS} max).

For all practical purposes, eGaN FETs can be operated within datasheet limits without any concern about failure from any intrinsic gate failure mechanism. This is also supported by the lack of any field returns for gate failures for several years and over many billions of hours of usage in the field. It is important to remember, however, that this kind of acceleration study only provides insight into intrinsic (or fundamental) device failure modes. Extrinsic failure modes (i.e. random defects) may occur at very low levels, causing the failure rate at low voltage to be higher than predicted by this acceleration study. The only valid method to quantify extrinsic failure modes is to conduct large sample size studies such as Early Life Failure Rate (ELFR). In our Phase 8 report [8], we reported on ELFR testing under HTGB stress for 48 hours using a large population of parts. This experiment put an upper bound (60% confidence) on the extrinsic failure rate of < 220 ppm. In addition, based on the total number of eGaN® FETs in the field, with zero field failures for gate breakdown, we calculate an upper bound at << 1 ppm.

CONCLUSIONS

eGaN® devices have been in volume production for over 9 years and have demonstrated very high reliability in both laboratory testing and customer applications such as lidar for autonomous cars, 4G base stations, vehicle headlamps, and satellites to name just a few. In the first section of this Phase 10 report, the results of automotive AEC-Q101 qualification were shown. This achievement demonstrates the maturity and basic reliability of eGaN technology. Section 2 explored the extremes of dynamic $R_{DS(on)}$ testing during hard-switching conditions and demonstrated that eGaN® devices are stable over long term continuous switching operation. These tests also confirmed that hot carrier scattering into surface traps is the primary physical origin of dynamic $R_{DS(on)}$ shifting. Section 3 revisited gate reliability and reaffirmed what customers have already discovered: eGaN FET gates are very rugged and reliable. The dominant intrinsic failure mechanism was found to be abrupt gate rupture (similar to TDDB), which is strongly voltage accelerated and only weakly temperature dependent.

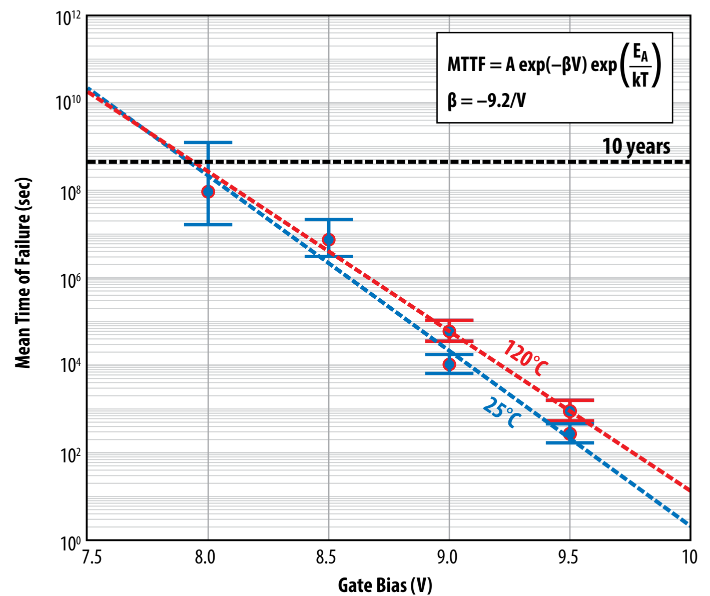


Figure 8: Mean time to failure (MTTF) versus gate bias and temperature. 25°C data is indicated in blue, and 120°C in red. Error bars on each data point indicate 90% confidence intervals on the MTTF resulting from the MLE Weibull fit. Dashed lines indicate best fit to a conventional exponential voltage acceleration function (characterized by parameters A and β shown in the equation). A separate fit was performed at both temperatures.

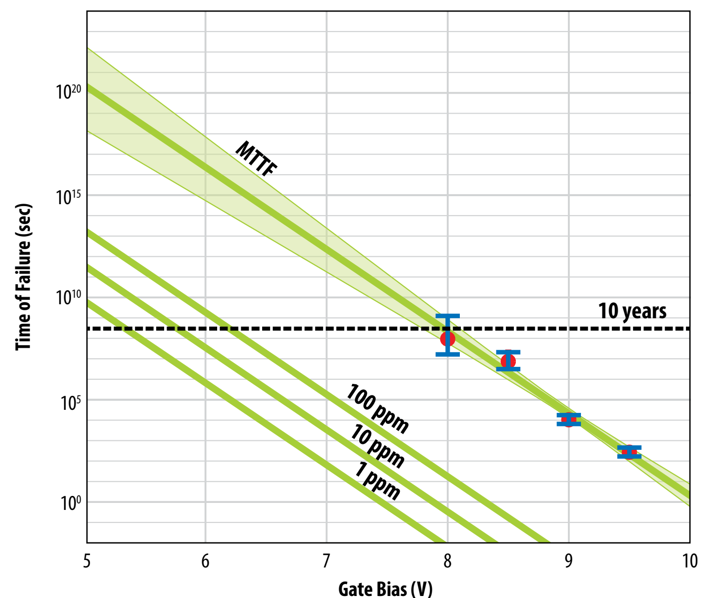


Fig 9: Mean time to failure (MTTF) and time to X ppM failure (T_{XppM}) versus gate bias at 25°C. Green solid lines are the best fit to the exponential acceleration function, and the shaded area represents the 90% confidence interval on the 2-parameter fit.

APPENDIX A: SUMMARY OF QUALIFICATION TEST RESULTS

Stress Test	Sample Quantity	Equivalent Device (hrs)	Fail Quantity	Upper Bound Failure Statistics (60% Confidence)	Notes
HTRB	5102	5121960	0	179 FIT (637yrs)	$V_{DS} \geq 80\% V_{DS}$ Max
HTGB	4639	5705360	0	160 FIT (713yrs)	$V_{GS} \geq 5.5V$
H3TRB	2388	2308960	0	397 FIT (287yrs)	$V_{DS} = 80\% V_{DS}$ Max
ELFR_HTRB	11406	2460528	0	140 ppm	ELFR (48 hrs) and HTRB $V_{DS} \geq 80\% V_{DS}$ Max
ELFR_HTGB	7393	2703344	0	218 ppm	ELFR (48 hrs) and HTGB $V_{GS} \geq 5.5V$
All Tests	**30928**	**18300152**	**0**		

Table A.1: Summary of Qualification Test Results

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